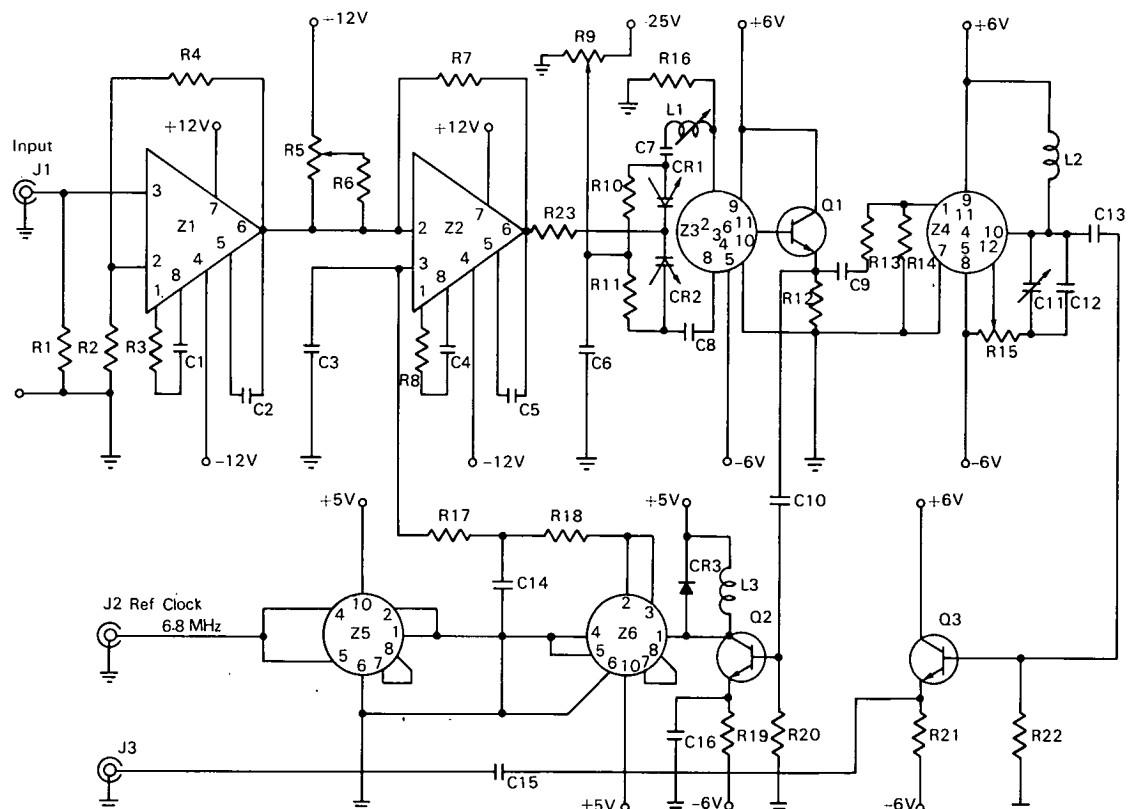


NASA TECH BRIEF



NASA Tech Briefs are issued to summarize specific innovations derived from the U.S. space program, to encourage their commercial application. Copies are available to the public at 15 cents each from the Clearinghouse for Federal Scientific and Technical Information, Springfield, Virginia 22151.

Phase-Locked-Loop Phase Modulator with High Modulation Index, Low Distortion



The circuit schematic shows a phase-locked-loop phase modulator that has the capability of generating a 6.8MHz carrier at modulation indexes as high as 2.5, with a distortion of the demodulated signal of less than 5 percent. These characteristics are obtained without the use of multipliers.

The phase-locked loop consists of Z3, Q1, Q2, Z6, and Z. The voltage-controlled oscillator, Z3, is associated with the frequency-determining voltage-variable capacitors CR1, CR2, and variable inductance L1. Blocking capacitors C7 and C8 are of sufficiently

large capacitance to prevent detuning of the tank circuit. Capacitors CR1 and CR2 receive a -12V bias from R9. Resistors R10 and R11, which are return paths for the bias voltage, prevent loading of the tuned circuit. The output stage of Z3 is an emitter follower which is connected to Q1 to allow capacitive-coupled loading at full output swing. Transistor Q2 converts the sinusoidal input (2.2 V, p-p) from Q1 into a 30-nsec-wide pulse going from +5.5 V to ground potential. (Diode CR3 is used to clamp the flyback at 5.5 V.) This pulse is directly coupled from the collector of

(continued overleaf)

Q2 to pin 1 of Z6. The latter is a pulse-triggered binary micrologic integrated circuit (connected to form a flip-flop) which serves as the phase detector of the phase-locked loop. The reference clock signal (6.8 MHz) entering Z5 at pins 4 and 5 is divided by 2, so that the frequency of the output square wave at pins 2 and 3 of Z5 is 3.4 MHz. This output is capacitively coupled to pins 4 and 5 of Z6, using the negative-going edge for triggering. The output of the phase detector, Z6, is taken from pins 2 and 3 and fed into a low-pass filter network consisting of R18, C14, R17, and C3. This filter reduces the 3.4 MHz fundamental frequency originating at output pins 2 and 3 of the phase detector, Z6. Resistors R17 and R18 also provide a dc return for Z2. The output of the low-pass filter feeds into pin 2, the noninverting side of Z2. The amplified correction voltage from pin 6 of Z2 is fed back through R23 to CR1 and CR2.

The modulation signal is injected at J1 into the noninverting input of Z1 at pin 3 (approximately 20,000 ohm input impedance). With a 1 V p-p input signal at J1, the amplifier (Z1) has a gain of 5; its frequency response is flat out to 100 kHz and rises by 1.0 dB at a frequency of 330 kHz. This amplifier has the important function of providing a dc-coupled modulating signal to Z2 so that the low frequency response of the modulator is unrestricted. The amplifier also provides a virtual ground for R5 and compensates for the loss of modulation signal through this resistor, which furnishes a dc offset voltage at pin 2 of Z2. Phase modulation occurs when the modulation signal enters this pin. As Z3 is phase-locked to the reference signal at J2, the demodulated signal originating at the phase detector (Z6) output cancels any changes in frequency of the voltage-controlled oscillator (Z3) that would be caused by the amplified modulation signal from Z2. This cancellation will occur at pin 6 of Z2 and depends on the loop gain and phase shift through the loop. As the modulation frequency is increased, the signal at this pin increases in lead until the first break point of the closed-loop response is reached.

Theoretically, this circuit can have a maximum phase deviation of 180° (modulation index of 3.14), but in actual practice this deviation is limited by (1) the capability of the phase detector, Z6, to produce a properly damped, full square wave at the reference frequency, and (2) the loss in pulse width of the Z6 square wave output at the dc switching level of the pulse input to pin 1 of Z6. The large phase deviations of this circuit are made possible by the use of Z6, which is a digital-type (variable duty cycle) phase detector.

Values and types of components designated in the schematic are listed below. All resistors are rated at

$1/4$ W; resistance values are given in K ohms unless indicated as ohms. Designation of commercial company products is only indicative, not exclusive, and is not a recommendation of one company over another.

| | |
|------------------|--------------------------------------|
| R1, R2 | = 22 |
| R3, R8, R20 | = 1.5 |
| R4 | = 82 |
| R5 | = 10 |
| R6, R23 | = 3.3 |
| R7 | = 5.6 |
| R9 | = 10 (Pot.) |
| R10, R11 | = 15 |
| R12 | = 100 |
| R13 | = 33 |
| R14 | = 2.2 ohms |
| R15 | = 5 (Pot.) |
| R16 | = 68 ohms |
| R17 | = 8.2 |
| R18, R19 | = 1.8 |
| R21 | = 180 ohms |
| R22 | = 1 |
| C1, C4 | = 270 pf (mica) |
| C2 | = 18 pf |
| C3 | = 22 pf |
| C5 | = 20 pf |
| C6-C10, C13, C15 | = 0.022 μ f |
| C11 | = 0.8-18 pf |
| C12 | = 39 pf |
| C14 | = 82 pf |
| Z1, Z2 | = Fairchild μ a 709 |
| Z3 | = RCA CA-3001 |
| Z4 | = RCA CA-3005 |
| Z5, Z6 | = Fairchild Dt μ l 950 |
| Q1, Q3 | = 2N 2222 |
| Q2 | = 2N 2369 |
| L1 | = Cambion 1505-5 7.8 - 16 μ H |
| L2, L3 | = 10 μ H |
| CR1, CR2 | = TRW varicap 1N 4815B |
| CR3 | = 1N914 |

Note:

This Tech Brief is complete in itself. No additional information is available.

Patent status:

No patent application is contemplated by NASA.

Source: C. G. Badstibner of
Radio Corporation of America
under contract to
Manned Spacecraft Center
(MSC-12247)